CLAIMS

What is claimed is:

1. A system, comprising:

a first processor that executes a transaction targeting a pre-determined address;

a second processor coupled to said first processor; and

a wait unit coupled to said first and second processors, said wait unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode.

2. The system of claim 1 wherein the wait signal is de-asserted to permit the first processor to retrieve a status of the second processor.

3. The system of claim 2 wherein said status includes one or more instructions that the first processor is to execute.

4. The system of claim 1 wherein said transaction comprises a read instruction.

5. The system of claim 1 wherein said transaction comprises a write instruction.

6. The system of claim 1 wherein said wait unit de-asserts the wait signal upon detection of a system interrupt signal generated by the first processor.

7. The system of claim 1 wherein said wait unit de-asserts the wait signal upon detection of a signal from said second processor.

8. The system of claim 7 wherein said wait unit upon detection of said signal asserts a processor interrupt signal to the first processor if the wait signal is already de-asserted.

9. A method, comprising:

executing a transaction that targets a pre-determined address;

detecting the transaction to said pre-determined address;

asserting a wait signal upon detection of the transaction to cause a processor to stall;

causing said wait signal to de-assert upon occurrence of an event, said de-assert controlled by logic external to said processor.

10. The method of claim 9 wherein said stall comprises a low power mode.

11. The method of claim 9 wherein said event comprises a system interrupt.

12. The method of claim 9 wherein said event comprises a signal from another processor.

13. The method of claim 9 wherein said transaction is a read instruction to said pre-determined address.

14. The method of claim 9 wherein said transaction is a write instruction to said pre-determined address.

15. A wait unit, comprising:

a decode logic unit that determines when a first processor runs a transaction to a pre-determined address;

a first processor interface;

a second processor interface;

logic coupled to the decode logic unit, the first processor interface, and the second processor interface, wherein said logic asserts a signal propagated by the first processor interface to cause said processor to stall.

16. The wait unit of claim 15 wherein said transaction is a read instruction.

17. The wait unit of claim 15 wherein said transaction is a write instruction.

18. The wait unit of claim 15 wherein said second processor interface receives a wait release signal from a second processor that causes the wait unit to de-assert the wait signal to said first processor through said first processor interface.

19. The wait unit of claim 18 wherein said wait release signal causes a processor interrupt signal to be asserted if the wait signal is already de-asserted.

20. The wait unit of claim 15 further comprising a system interrupt interface coupled to the logic, through which a system interrupt signal is received that causes the logic to de-assert said wait signal to said first processor through the first processor interface.

21. A system, comprising:

a first processor;

a second processor;

means for detecting a transaction targeting a pre-determined address and for asserting a wait signal to said first processor to cause the first processor to enter a wait state; and

means for releasing said first processor from the wait state.

22. The system of claim 21 wherein the transaction comprises a memory read.

23. The system of claim 21 wherein the transaction comprises a memory write.

24. The system of claim 21 wherein said means for releasing said first processor from the wait state comprises a wait release signal from said second processor coupled to a wait unit, said wait unit de-asserts the wait signal upon detection of the wait release signal.

25. The system of claim 21 wherein said means for releasing said first processor from the wait state comprises a system interrupt signal to a wait unit, said wait unit de-asserts the wait signal upon detection of the system interrupt signal.